ABSTRACT OF THE DISCLOSURE

A data recovery apparatus for minimizing errors due to clock skew and a data recovery apparatus therefor are provided. The data recovery apparatus comprises a phase locked loop (PLL), an oversampler, a level transition detector, a transition accumulator, a state selector, and a data selector. The PLL generates a plurality of phase clock signals having different delay times, which signals are synchronized with an input clock signal. The oversampler 110 M (>1) times oversamples data serially input from the outside in response to the plurality of phase clock signals and outputs the oversampled result as a plurality of bit data items. The level transition detector receives the plurality of bit data output from the oversampler, detects the point of time at which the level transitions between adjacent bits and outputs the detection result as first through Mth transition signals. The transition accumulator accumulates the number of generations of the first through Mth transition signals output from the level transition detector and outputs a signal whose generation frequency is high as first through Mth transition accumulation signals. The state selector generates a state signal for selecting bit data items of corresponding positions among the plurality oversampling data items in response to the first through Mth transition accumulation signal. The data selector receives the oversampled plurality of bit data, selects bit data items of the sampling positions corresponding to the state signal, and outputs the selected bit data items in parallel. It is possible to minimize errors due to clock skew, which can be generated during the reproduction of data.